Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 55-78 and 85-89 are pending in the Application. Claims 55-66, 72-74 and 85-89 have been canceled in order to put the Application in condition for allowance. Claim 69 has been amended to correct a typographical error. Two new dependent claims, 90 and 91, are presented.

Listing of Claims:

Claims 1-54 (Previously canceled).

Cancel claims 55-65.

66. (Previously Presented) A system comprising:

a connector to a bus;

an instruction memory to store a bus stimuli instruction, the instruction having a predefined length, the instruction containing a plurality of segments, the plurality of segments including at least a flow segment and a data segment;

a logic device coupled with the instruction memory to receive the bus stimuli instruction and generate digital logic based on the bus stimuli instruction, the logic device comprising a flow portion, a request portion, and a data portion, the flow portion to receive at least the flow segment from the instruction memory, and the data portion to receive at least the data segment from the instruction memory, the flow portion, the request portion, and the data portion each

comprising a device selected from the group consisting of a field programmable gate array and an application specific integrated circuit;

a plurality of phase engines coupled between the logic device and the connector to translate the digital logic into signals and provide the signals to the bus, the plurality of phase engines including a system phase engine, an arbitration phase engine, a request phase engine, a snoop/error phase engine, and a data phase engine, the system phase engine, the arbitration phase engine, and the request phase engine coupled with the flow portion, the snoop/error phase engine coupled with the request portion, the data phase engine coupled with the data portion;

further comprising a response memory coupled with the flow portion and the request portion to store response information; and

further comprising a data memory coupled with the data portion to store data.

67. (Previously Presented) The system of claim 66, further comprising an interface to a computer to receive the bus stimuli instruction.

68. (Previously Presented) The system of claim 66, wherein the bus stimuli instruction is based on an existing simulation stimulus software.

69. (Currently Amended) A system comprising:

a containing a file that is based on an existing simulation stimulus software and that contains a plurality of bus stimuli instructions that represent a predefined sequence of bus transactions, wherein each transaction has a plurality of transaction phases;

a processor bus;

a transaction generator containing a first connector coupled to the computer to receive the file and containing a second connector coupled to the bus to provide a plurality of bus compatible signals to the bus, the transaction generator further containing:

an instruction memory to store the file; and

one or more phase generators coupled with the instruction memory to receive the plurality of bus stimuli instructions and to generate the plurality of bus compatible signals that represent the predefined sequence of bus transactions,

wherein the one or more phase generators includes a logic device selected from the group consisting of a [flow] field programmable gate array and an application specific integrated circuit to implement the instructions as digital logic, and

wherein the one or more phase generators include a translation device coupled between the logic device and the bus to translate the digital logic to the plurality of bus compatible signals; and

a component selected from the group consisting of a processor and a chipset coupled to the bus to respond to the plurality of bus compatible signals.

70. (Previously Presented) The system of claim 69, further comprising a logic analyzer coupled with the bus to capture information associated with the response of the component to the plurality of bus compatible signals.

71. (Previously Presented) The system of claim 69, wherein the plurality of bus stimuli instructions are based on a high level language.

Cancel Claims 72-74.

75. (Previously Presented) A method comprising:

coupling a component to a bus;

coupling a device comprising an instruction memory and a phase generator to the bus;

storing a plurality of instructions representing a predefined sequence of bus transactions in the instruction memory;

providing the plurality of instructions from the instruction memory to the phase generator;

using the phase generator to provide signals representing the predefined sequence of bus transactions to the bus based on the plurality of instructions; and

detecting a bug of the component by determining an incorrect response of the component to the predefined sequence of bus transactions.

76. (Previously Presented) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a processor.

77. (Previously Presented) A component designed to eliminate a bug detected by the method of claim 75, wherein the component comprises a chipset.

78. (Previously Presented) The method of claim 75, further comprising specifying the plurality of instructions in a high level language.

Claims 79-84 (Previously Canceled) .

Cancel Claims 85-89.

90. (New) The method of claim 75, further comprising deriving the plurality of instructions from at least one selected from a bus functional model, simulation, and logic analyzer trace file.

91. (New) The method of claim 75, further comprising repeating using the phase generator to provide signals representing the predefined sequence of bus transactions to the bus in order to stress the bus.